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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Ihida, et al.

Serial No.: 09/695,212 Group Art Unit: 2871

Filed: October 25, 2000 Examiner: Prasad R. Akkapeddi

For: ACTIVE MATRIX LCD PANEL

Honorable Commissioner of Patents
Alexandria, Virginia 22313-1450

SUBMISSION OF VERIFIED TRANSLATION OF THE PRIORITY DOCUMENT

Sir:

Applicants hereby submit a verified translation of the priority document.

Respectfully Submitted,

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CERTIFICATION

I, Harumasa ISHIZAKI of FUSOH PATENT FIRM, Rindo Building, 5F, 37, Kanda-Higashimatsushita-cho, Chiyoda-ku, Tokyo, 101 Japan, hereby certify that I am the translator of the accompanying certified official copy of the patent application No.11-304682 for a patent filed in Japan on October 26, 1999 and certify that the following is a true and correct translation to the best of my knowledge and belief.

Dated this 19th day of August 2003

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PATENT OFFICE

JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this Office.

DATE OF APPLICATION October 26, 1999

APPLICATION NUMBER Heisei 11th Patent Application No.304682

APPLICANT(S) NEC Corporation

NEC Kagoshima Ltd.

DATE July 14, 2000

Commissioner,

Patent Office Kozo OIKAWA

Certificate No. Patent-2000-3055261

[NAME OF DOCUMENT] APPLICATION FOR PATENT

[SERIAL NO.] 74610393

[DATE OF FILING] October 26, 1999

[ADDRESSEE] Commissioner, Patent Office

[INTERNATIONAL PATENT CLASSIFICATION] H01L 29/78

G02F 1/133

G09F 9/30

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[OFFICIAL FEE]

[PREPAYMENT NUMBER] 030362

[AMOUNT OF PAYMENT] 21,000Yen

[LIST OF DOCUMENTS ATTACHED]

[NAME OF DOCUMENT] SPECIFICATION.....1

[NAME OF DOCUMENT] DRAWINGS.....1

[NAME OF DOCUMENT] ABSTRACT.....1

[GENERAL POWER OF ATTORNEY NUMEBR] 9304371

[NAME OF DOCUMENT] Power of Attorney

[Supplemental Document] General power of attorney submitted on October 26, 1999 will be applied.

[REQUEST OF PROOF] REQUESTED

[Document Name] Specification

[Name of the Invention] ACTIVE MATRIX SUBSTRATE AND METHOD FOR FABRICATING THE SAME

[Claims]

[Claim 1] An active matrix substrate comprising a gate electrode having a transparent electrode and a metal film stacked in layers in that order on a transparent insulative substrate, wherein

a gate insulating film formed so as to cover said gate electrode and an amorphous silicon semiconductor layer arranged on said gate insulating film are formed so as to generally overlap each other when viewed in a normal direction to the substrate,

said amorphous silicon semiconductor layer and a source/drain electrode are connected to each other via an opening provided on a passivation film covering a surface and sidewalls of said amorphous silicon semiconductor layer, and

said source electrode is connected to a pixel electrode formed in the same layer as said gate electrode by removing only said metal film of said transparent electrode and said metal film stacked in layers.

[Claim 2] An active matrix substrate comprising a gate electrode having a transparent electrode and a metal film stacked in layers in that order on a transparent insulative substrate, wherein

a gate insulating film formed so as to cover said gate electrode and an amorphous silicon semiconductor layer arranged on said gate insulating film are formed so as to generally overlap each other

when viewed in a normal direction to the substrate,

said amorphous silicon semiconductor layer and a source/drain electrode are connected to each other via an opening provided on a passivation film covering a surface and sidewalls of said amorphous silicon semiconductor layer,

said source electrode is connected to a pixel electrode formed in the same layer as said gate electrode by removing only said metal film of said transparent electrode and said metal film stacked in layers, and

said pixel electrode is provided with a storage capacitive portion having said passivation film sandwiched between a capacitive storage electrode formed in the same layer as said gate electrode and an opposing electrode formed in the same layer as said source electrode.

[Claim 3] An active matrix substrate comprising a gate electrode and a common electrode on a transparent insulative substrate, wherein

a gate insulating film formed so as to cover said gate electrode and an amorphous silicon semiconductor layer arranged on said gate insulating film are formed so as to generally overlap each other when viewed in a normal direction to the substrate, and

said amorphous silicon semiconductor layer and a source/drain electrode are connected to each other via an opening provided on a passivation film covering a surface and sidewalls of said amorphous silicon semiconductor layer.

[Claim 4] The active matrix substrate according to any one of claims

1 to 3, wherein

a phosphorus-doped n^+ layer is formed on a surface of the amorphous silicon semiconductor layer exposed in said opening, and said source/drain electrode of only metal is directly connected to said n^+ layer.

[Claim 5] The active matrix substrate according to any one of claims 1 to 4, wherein

said passivation film is formed in a layered structure having an organic interlayer film deposited on a silicon nitride film, said organic interlayer film being formed of any of acrylic resin, BCB (Benzocyclobutene), and polyimide as a material.

[Claim 6] The active matrix substrate according to any one of claims 1 to 4, wherein

said passivation film is formed in a layered structure having a silicon oxide film deposited on a silicon nitride film.

[Claim 7] A method for fabricating an active matrix substrate comprising at least the steps of:

(a) stacking a transparent electrode and a metal film in that order in layers on a transparent insulative substrate to form a gate electrode, a gate conductor trace, and a pixel electrode using a first mask;

(b) stacking a gate insulating film and an amorphous silicon semiconductor layer in layers on said gate electrode to form the gate insulating film and the amorphous silicon semiconductor layer in a predetermined shape using a second mask;

(c) depositing a passivation film so as to cover a surface and sidewalls of said amorphous silicon semiconductor layer to form an opening, passing through said passivation film, for connecting to a source/drain electrode, at a predetermined position on said amorphous silicon semiconductor layer using a third mask, while forming an opening, passing through said passivation film and said metal film, for exposing said metal oxide film, on said pixel electrode; and

(d) depositing an electrode layer on said passivation film and the opening to form a conductor trace for connecting between an amorphous silicon layer exposed in an opening for said source electrode and said pixel electrode using a fourth mask, while forming a drain conductor trace to be connected to the amorphous silicon layer exposed in the opening for said drain electrode.

[Claim 8] A method for fabricating an active matrix substrate comprising at least the steps of:

(a) depositing a metal film on a transparent insulative substrate to form a gate electrode, a gate conductor trace, and a common electrode conductor trace using a first mask;

(b) stacking gate insulating film and an amorphous silicon semiconductor layer in layers on said gate electrode to form the gate insulating film and the amorphous silicon semiconductor layer in a predetermined shape using a second mask;

(c) depositing a passivation film so as to cover a surface and sidewalls of said amorphous silicon semiconductor layer to form

an opening, passing through said passivation film, for connecting to a source/drain electrode, at a predetermined position on said amorphous silicon semiconductor layer using a third mask; and

(d) depositing an electrode layer on said passivation film and the opening to form a drain conductor trace to be connected to the amorphous silicon layer exposed in the opening for said drain electrode, using a fourth mask.

[Claim 9] A method for fabricating an active matrix substrate comprising at least the steps of:

(a) depositing a metal film on a transparent insulative substrate to form a gate electrode, a gate conductor trace, and a common electrode conductor trace using a first mask;

(b) stacking a gate insulating film and an amorphous silicon semiconductor layer in layers on said gate electrode to form only said amorphous silicon semiconductor layer in a predetermined shape using a second mask;

(c) depositing a passivation film so as to cover a surface and sidewalls of said amorphous silicon semiconductor layer to form an opening, passing through said passivation film, for connecting to a source/drain electrode, at a predetermined position on said amorphous silicon semiconductor layer using a third mask; and

(d) depositing an electrode layer on said passivation film and the opening to form a drain conductor trace to be connected to the amorphous silicon layer exposed in the opening for said drain electrode.

[Claim 10] The method for fabricating an active matrix substrate according to any one of claims 7 to 9, wherein

said electrode layer deposited in said step (d) is formed in a layered structure having a amorphous silicon layer doped with an impurity and a metal layer deposited in that order.

[Claim 11] The method for fabricating an active matrix substrate according to any one of claims 7 to 9, further comprising the steps of:

after said step (c) of forming an opening in the passivation film and before said step (d) of forming the electrode layer, doping with phosphorus said amorphous silicon semiconductor layer exposed in said opening to form an n^+ layer on a layer surface while holding said transparent insulative substrate in a PH_3 gas atmosphere, wherein

said electrode layer formed of only a metal layer is connected to said n^+ layer.

[Claim 12] The method for fabricating an active matrix substrate according to any one of claims 7 to 11, wherein

said passivation film is formed in a layered structure having an organic interlayer film deposited on a silicon nitride film, said organic interlayer film being formed of any of acrylic resin, BCB (Benzocyclobutene), and polyimide as a material.

[Claim 13] The method for fabricating an active matrix substrate according to any one of claims 7 to 11, wherein

said passivation film is formed in a layered structure having a silicon oxide film deposited on a silicon nitride film.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to an active matrix substrate and a method for fabricating the substrate, and more particularly, to a channel protective type active matrix substrate having a channel protective film formed on a surface of an amorphous silicon semiconductor layer and a method for fabricating the substrate.

[0002]

[Prior Art]

An active matrix liquid crystal display device employing active elements such as thin film transistors features being thin and light in weight and is utilized as a flat panel display of high image quality. The liquid crystal display device employs a vertical electric field (Twisted Nematic (TN)) system for driving liquid crystal, which is sandwiched between two substrates having transparent electrodes formed thereon, at a voltage applied between the transparent electrodes, or a horizontal electric field system for driving the liquid crystal using interdigitated pixel electrodes having a liquid crystal layer sandwiched therebetween. In any of these systems, studies have been conducted on how to simplify the process for fabricating the active matrix substrate in order to achieve a low cost.

[0003]

As shown in Fig. 1, in general, the active matrix substrate

according to the TN system includes gate conductor traces 12 and drain conductor traces 14 extending orthogonal to each other, pixel electrodes 10 each formed within a region surrounded by these conductor traces, and thin film transistors (TFT) 17 each formed near an intersection of a gate conductor trace and a drain conductor trace, with a channel protective film for ensuring performance being formed on a surface of the thin film transistor 17. There is formed an alignment film (not shown) for aligning liquid crystal in a predetermined direction on the thin film transistor 17 and the pixel electrode 10 of the active matrix substrate, and liquid crystal is sealed between the alignment film and an opposing substrate having a color filter, a common electrode, and the alignment film formed thereon, thereby forming a liquid crystal display device.

[0004]

A typical method for fabricating such an active matrix substrate will be described below. First, an ITO (Indium Tin Oxide) is deposited on a transparent insulative substrate to form a patterned resist using a first photomask, and the exposed ITO is etched to form pixel electrodes. Subsequently, a metal film such as of Cr, Mo, or Al, serving as gate electrodes, is deposited on the transparent insulative substrate to form a patterned resist using a second photomask, and the exposed metal film is etched to form gate electrodes.

[0005]

Then, a gate insulating film such as of SiNx is deposited so

as to cover the gate electrode to provide an opening at a predetermined position using a third photomask, and thereafter amorphous silicon (hereinafter referred to as "a-Si") is deposited to selectively etch the a-Si using a fourth photomask and thereby form an island-shaped a-Si layer. Then, a channel protective film such as of SiNx is deposited on the a-Si layer, and the channel protective film is etched using a fifth photomask so that the channel protective film remains on the position of the channel on the a-Si layer.

[0006]

Then, to provide an ohmic contact with the a-Si layer, an n^+ a-Si doped with an impurity is deposited and then a metal such as Cr, Mo, or Al is deposited to form source/drain electrodes using a sixth photomask. Fabrication of an active matrix substrate by the method requires processing using a total of six masks, and thus various fabrication methods have been suggested to reduce the steps in number.

[0007]

For example, as those fabrication methods, the invention described in Japanese Patent Laid-Open Publication No. Sho 63-218925 is explained below with reference to Fig. 13. Fig. 13 is a schematic sectional view illustrating the steps of a method for fabricating a prior art TN active matrix substrate, in which the left side in the figure indicates a gate terminal portion and the center indicates a pixel portion.

[0008]

The active matrix substrate described in the publication is constructed as follows. First, as shown in Fig. 13(a), ITO and a metal film such as of Cr, Mo, or Al are successively deposited by sputtering on a transparent insulative substrate 1 to form a patterned resist using a first photomask, and the exposed ITO and the metal film are etched to simultaneously form gate electrodes 2 and pixel electrodes 10.

[0009]

Then, as shown in Fig. 13(b), a gate insulating film 4 such as of SiNx, an intrinsic a-Si layer 5, and a channel protective film 25 such as of SiNx are successively deposited. Thereafter, using a second photomask, an unnecessary channel protective film 25 is selectively etched so as to form the channel protective film 25 at the channel region of the intrinsic a-Si layer 5.

[0010]

Then, as shown in Fig. 13(c), an ohmic contact layer 6 of an n^+ a-Si doped with an impurity is deposited. Then, using a third photomask, the ohmic contact layer 6, the intrinsic a-Si layer 5, the gate insulating film 4, and an upper gate metal film are collectively etched to expose the ITO at the drawing portions of the pixel electrode 10 and the gate electrode 2.

[0011]

Then, as shown in Fig. 13(d), a source/drain metal film such as of Al is deposited. Then, using a fourth photomask, the source/drain metal film on the channel region and the ohmic contact

layer 6 are selectively etched, while the source/drain metal film is formed in a predetermined shape, thereby completing the fabrication of the active matrix substrate.

[0012]

[Problems to be Solved by the Invention]

According to the method described in the publication, it is possible to use only four masks to fabricate an active matrix substrate which has the channel protective film 25 formed on the channel region at the upper portion of the intrinsic a-Si layer 5. However, after the channel protective film 25 is formed, the ohmic contact layer 6, the intrinsic a-Si layer 5, the gate insulating film 4, and the upper gate metal film are collectively etched in the step of Fig. 13(c), thereby raising a problem that the side surfaces of the intrinsic a-Si layer 5 are not covered with the channel protective film 25 but exposed.

[0013]

In the case where the sidewalls of the intrinsic a-Si layer 5 is not covered with the channel protective film 25 of a dense material such as SiNx as described above, the liquid crystal layer exists only via a coarse film such as a polyimide alignment film. This may allow impurities present in the liquid crystal layer to enter the intrinsic a-Si layer 5 due to diffusion or electric fields, resulting in a significant degradation in TFT properties. To avoid this problem, the currently available active matrix substrate is constructed such that a passivation film is coated after the step

of Fig. 13(d) to cover the side surfaces of the intrinsic a-Si layer 5. In this case, since an opening is provided to the gate terminal, the drain terminal, and the pixel electrode, a fifth mask has to be employed. Accordingly, this raises a problem that an additional step for one PR ruins man-hour reduction effects after all.

[0014]

The present invention was developed in view of the problems. It is therefore a principal object of the invention to provide an active matrix substrate and its fabrication method, by which only four masks are employed to form a channel protective type active matrix substrate with the entire surface of an a-Si layer being covered with passivation film.

[0015]

In order to achieve the above object, first aspect of the present invention is to provide an active matrix substrate comprising a gate electrode having a transparent electrode and a metal film stacked in layers in that order on a transparent insulative substrate, wherein

a gate insulating film formed so as to cover said gate electrode and an amorphous silicon semiconductor layer arranged on said gate insulating film are formed so as to generally overlap each other when viewed in a normal direction to the substrate,

said amorphous silicon semiconductor layer and a source/drain electrode are connected to each other via an opening provided on a passivation film covering a surface and sidewalls of said amorphous silicon semiconductor layer, and

said source electrode is connected to a pixel electrode formed in the same layer as said gate electrode by removing only said metal film of said transparent electrode and said metal film stacked in layers.

[0016]

Second aspect of the present invention is to provide an active matrix substrate comprising a gate electrode having a transparent electrode and a metal film stacked in layers in that order on a transparent insulative substrate, wherein

a gate insulating film formed so as to cover the gate electrode and an amorphous silicon semiconductor layer arranged on the gate insulating film are formed so as to generally overlap each other when viewed in a normal direction to the substrate,

the amorphous silicon semiconductor layer and a source/drain electrode are connected to each other via an opening provided on a passivation film covering a surface and sidewalls of the amorphous silicon semiconductor layer,

the source electrode is connected to a pixel electrode formed in the same layer as the gate electrode by removing only the metal film of the transparent electrode and the metal film stacked in layers, and

the pixel electrode is provided with a storage capacitive portion having the passivation film sandwiched between a capacitive storage electrode formed in the same layer as the gate electrode and an opposing electrode formed in the same layer as the source

electrode.

[0017]

According to the present invention, the active matrix substrate wherein a phosphorus-doped n^+ layer is formed on a surface of the amorphous silicon semiconductor layer exposed in the opening, and the source/drain electrode of only metal is directly connected to the n^+ layer.

[0018]

Third aspect of the present invention is to provide a method for fabricating an active matrix substrate comprising at least the steps of:

(a) stacking a transparent electrode and a metal film in that order in layers on a transparent insulative substrate to form a gate electrode, a gate conductor trace, and a pixel electrode using a first mask;

(b) stacking a gate insulating film and an amorphous silicon semiconductor layer in layers on the gate electrode to form the gate insulating film and the amorphous silicon semiconductor layer in a predetermined shape using a second mask;

(c) depositing a passivation film so as to cover a surface and sidewalls of the amorphous silicon semiconductor layer to form an opening, passing through the passivation film, for connecting to a source/drain electrode, at a predetermined position on the amorphous silicon semiconductor layer using a third mask, while forming an opening, passing through the passivation film and the

metal film, for exposing the metal oxide film, on the pixel electrode; and

(d) depositing an electrode layer on the passivation film and the opening to form a conductor trace for connecting between an amorphous silicon layer exposed in an opening for the source electrode and the pixel electrode using a fourth mask, while forming a drain conductor trace to be connected to the amorphous silicon layer exposed in the opening for the drain electrode.

[0019]

[Embodiments of the Invention]

An active matrix substrate according to the present invention is fabricated in a preferred embodiment as follows. That is, a transparent electrode and a metal film are staked in layers on a transparent insulative substrate to form gate electrodes (2a, 2b in Fig. 3) and pixel electrodes using a first mask. On top thereof, a gate insulating film (4 in Fig. 3) and an intrinsic amorphous silicon layer (5 in Fig. 3) are stacked in layers and formed collectively in a predetermined shape using a second mask, so that passivation film (9 in Fig. 3) deposited so as to cover a surface and sidewalls of the intrinsic amorphous silicon layer is provided with an opening. On top thereof, electrode layers (7 and 8 in Fig. 3) are deposited to form predetermined conductor traces using a fourth mask. Thus, using only four masks, an active matrix substrate of a channel protective type is fabricated which has the intrinsic amorphous silicon layer covered completely with the passivation

film.

[0020]

[Embodiments]

To describe the embodiments of the present invention in more detail, the embodiments according to the present invention will be discussed below with reference to the drawings.

[0021]

[Embodiment 1]

First, referring to Figs. 1 to 4, described are a vertical electric field (TN) channel protective type active matrix substrate according to a first embodiment of the present invention and its fabrication method. Fig. 1 is a circuit diagram illustrating an active matrix substrate according to the first embodiment. Fig.2 is a plan view illustrating the fabrication steps of the active matrix substrate, with one pixel being extracted. Fig.3 is a sectional view illustrating the fabrication steps of the active matrix substrate, with the left side in the figure showing a gate terminal portion (a cross sectional view taken along the line A-A' of Fig. 1), the center showing a pixel portion (a cross sectional view taken along the line C-C' of Fig. 2), and the right side showing a drain terminal portion (a cross sectional view taken along the line B-B' of Fig. 1). Fig.4 is a sectional view illustrating the shape of a connection between a gate electrode and a drain conductor trace at gate storage and protective transistor portions, or the shape of a connection between a gate conductor trace and a source/drain

electrode.

[0022]

The active matrix substrate according to the first embodiment is a substrate for use with a vertical electric field (Twisted Nematic (TN)) liquid crystal display device which drives liquid crystal using an alignment film provided on the active matrix substrate and an alignment film provided on an opposing substrate, or a channel protective type active matrix substrate in which the upper and side surfaces of the intrinsic a-Si layer 5 constituting the TFT 17 are completely covered with the passivation film 9.

[0023]

A method for fabricating the active matrix substrate according to this embodiment will be described with reference to Figs. 2 and 3. First, as shown in Fig. 3(a), a transparent electrode (ITO) and a metal film such as of Cr, Ti, Mo, or Al are stacked in layers in that order on the transparent insulative substrate 1 such as glass, for example, by sputtering with the ITO being in a thickness of about 30 to 100nm and the metal film being in a thickness of about 0.1 to 0.3μm. Thereafter, using a mask having the shape as shown in Fig. 2(a), a patterned resist is formed on the region serving as the pixel electrode 10, the gate electrode 2, and the gate conductor trace 12, and then the metal film and the ITO present at the regions not covered with the patterned resist are removed by wet etching.

[0024]

Then, the gate insulating film 4 such as of SiNx and the intrinsic

a-Si layer 5 serving as a semiconductor layer are successively deposited on the entire surface of the transparent insulative substrate 1 by plasma CVD or the like. Preferably, the SiNx has a thickness of about 0.3 to 0.5μm and the a-Si has a thickness of about 0.05 to 0.2μm. After the deposition, using a second mask, a patterned resist is formed so as to cover the gate electrode, and an unnecessary intrinsic a-Si layer 5 and gate insulating film 4 are removed by dry etching, thereby providing the structure as shown in Fig. 3(b).

[0025]

Then, the passivation film 9 such as of SiNx serving as a channel protective film for the TFT 17 is deposited on the entire surface of the substrate 1 by plasma CVD, for example, in a thickness of about 0.1 to 0.4μm. Subsequently, a third mask having contact holes 11 at the source/drain junction on the intrinsic a-Si layer 5, the pixel electrode 10, a gate terminal 15, and a drain terminal 16 is used to form a patterned resist, and the exposed passivation film 9 is removed by dry etching or by wet etching. Subsequently, only the gate metal film of the pixel electrode 10, the gate terminal 15, and the drain terminal 16 is removed by dry etching or by wet etching, thereby providing the structure as shown in Fig. 3(c).

[0026]

Then, to provide an ohmic contact with the intrinsic a-Si layer 5, the ohmic contact layer 6 of an n^+ a-Si doped with an impurity is deposited by CVD, for example, in a thickness of 20 to 100nm.

Subsequently, a barrier film such as of Cr, Mo, or Ti serving as the source/drain electrodes 7, 8 and a metal film such as of Al are deposited by sputtering, for example, in a thickness of about 0.1 to 0.3μm.

[0027]

As a method for providing an ohmic contact with the a-Si layer, it is also possible to provide an ohmic contact between the intrinsic a-Si layer 5 and the source/drain electrodes 7, 8 by forming an opening in the passivation film 9 and then diffusing phosphorus into the intrinsic a-Si layer 5 to form an n^+ layer on the surface of the intrinsic a-Si layer 5 while holding the substrate in a PH_3 plasma atmosphere, in place of forming the ohmic contact layer 6. For example, as the processing conditions at that time, a plasma CVD device was used to supply a PH_3/H_2 gas (0.5% PH_3) at 1000sccm at a temperature of 300°C for processing at a pressure of 200Pa with an RF power of 0.1W/cm^2 for 5 minutes.

[0028]

Then, using a fourth mask, an unnecessary source/drain metal film is etched to connect between the source electrode 8 of the intrinsic a-Si layer 5 and the pixel electrode 10, thereby forming the drain conductor trace 14 to be connected to the drain electrode 7. Then, through oxygen plasma processing or a heat treatment in an oxidative atmosphere or the like, the surface of the drain conductor trace is oxidized. By such oxidation processing being performed, it is possible to prevent the occurrence of a trouble that electrically

conductive foreign particles present in the liquid crystal layer may cause the drain conductor trace and the common transparent electrode on the color filter to short-circuit due to a small mechanical shock. In this way, the active matrix substrate having the structure of Fig. 3(d) can be fabricated.

[0029]

As described above, the method for fabricating the active matrix substrate according to this embodiment makes it possible to employ only four masks to form a channel protective type active matrix substrate with the surface and sidewalls of the intrinsic a-Si layer 5 being completely covered with a dense passivation film 9 such as of SiNx. When compared with the prior art fabrication method, this method makes it possible to simplify the process by eliminating at least one PR. There may be a problem of causing display deficiencies such as display unevenness or the like due to deterioration in TFT property resulting from the intrinsic a-Si layer 5 being not covered with a dense passivation film; however, the present invention does not cause such a problem.

[0030]

Furthermore, since the gate insulating film is removed in the step of Fig. 3(c), the gate storage capacitor fabricated by the method according to this embodiment can be constructed such that only the passivation film 9 can be sandwiched between the electrode formed in the same layer as the gate electrode 2 and a gate storage electrode 21 formed in the same layer as the source electrode 8,

as shown in Fig. 4(a). Accordingly, the absence of the gate insulating film 4 makes it possible to provide a storage capacitance increased by that amount when compared with Fig. 13(a) illustrating the structure fabricated by the prior art method. That is, a higher opening ratio can also be achieved because a necessary capacitance value can be ensured even with a reduced area occupied by the storage capacitor.

[0031]

On the other hand, the active matrix substrate is provided with a protective element 18 for preventing electrostatic damage to the TFT between each drain conductor trace 14 and gate conductor trace 12. The protective element 18 that is formed in the same step as that for the TFT for driving the pixel includes a TFT, the gate electrode and the source/drain electrode of which are connected to the drain conductor trace 14 as well as the source/drain electrode of which are connected to the gate conductor trace 12, and a TFT, the gate electrode and the source/drain electrode of which are connected to the gate conductor trace 12 as well as the source/drain electrode of which are connected to the drain conductor trace 14. It is necessary to connect between the gate metal film and the source/drain metal film in order to make the protective element 18. To this end, the gate insulating film 4 is removed in the step of Fig. 3(c), and the ohmic contact layer 6 and the drain conductor trace 14 are formed in the step of Fig. 3(d), thereby allowing the drain conductor trace 14 and the gate conductor trace 12 to be

connected to each other at the ohmic contact layer 6, as shown in Fig. 4(b). That is, the protective element for preventing electrostatic damage to the TFT can also be formed with the four PRs remaining unchanged in number. Although the surfaces of the gate storage electrode 21 and the drain conductor trace 14 are also subjected to the oxidation simultaneously in the step described in paragraph [0028], the resulting oxide film is not illustrated in Fig. 4.

[0032]

[Embodiment 2]

Now, a channel protective type active matrix substrate according to a second embodiment of the present invention and its fabrication method will be described below with reference to Fig. 5. Fig.5 is a sectional view illustrating the fabrication steps of the active matrix substrate, with the left side in the figure showing a gate terminal portion (a cross sectional view taken along the line A-A' of Fig. 1), the center showing a pixel portion (a cross sectional view taken along the line C-C' of Fig. 2), and the right side showing a drain terminal portion (a cross sectional view taken along the line B-B' of Fig. 1). The second embodiment is different from the first embodiment in that organic interlayer film is formed on the passivation film 9 serving as a channel protective film so as to flatten the substrate, with the others such as the structure, material, thickness, and fabrication method being the same as those of the first embodiment.

[0033]

The method for fabricating the active matrix substrate according to the second embodiment will be described below. First, like in the first embodiment, using a first mask, formed on the transparent insulative substrate 1 are the gate electrode 2, the pixel electrode 10, an electrode having a layered structure of ITO and a metal such as Cr, Ti, Mo, or Al formed on the gate/drain terminals 15 and 16. After the gate insulating film 4 and the intrinsic a-Si layer 5 are stacked in layers, a pattern is formed using a second mask so that the gate insulating film 4 covers the gate electrode 2. Then, in the first embodiment, the passivation film 9 was formed in a thickness of 0.1 to 0.4μm required for protecting the channel. However, this embodiment is characterized in that an organic interlayer film 26 is further deposited on the passivation film 9 to simultaneously flatten the substrate.

[0034]

For example, the organic interlayer film may be made of an organic material such as acrylic resin, BCB (Benzocyclobutene), or polyimide, and these organic materials can be deposited in a thickness of about 0.2 to 0.1μm, thereby providing a flattened substrate as shown in Fig. 5(c). Provision of such an organic interlayer film 26 would make it possible to avoid a problem of causing the liquid crystal to be nonuniformly aligned due to the shoulders of the TFT 17.

[0035]

Although not illustrated, for example, other flattening methods include a method of forming a coarse film in quality by varying the conditions for depositing the passivation film 9 of SiNx such as the deposition rate or the deposition temperature, a method of forming a coarse SiNx film on a dense SiNx film in two-layer structure, or a method of stacking multiple films of different materials in layers, e.g., stacking SiO_2 or the like on a dense SiNx in layers.

[0036]

Now, the method of forming a SiO_2 film on a dense SiNx will be explained below. As the deposition conditions, like in the first embodiment, SiNx is deposited by CVD at a deposition rate of about 0.1μm/min in a thickness of about 0.1μm. Subsequently, SiO_2 is deposited by CVD at a deposition rate of about 0.5μm/min in a thickness of about 1μm. This makes it possible to form the passivation film 9 so as to fill in the shoulders at the edges of the intrinsic a-Si layer 5, thereby achieving the same effect as that provided by forming the organic interlayer film 26.

[0037]

When the deposition rate of the SiNx is modified, it is possible to achieve flatness not at a typical deposition rate of about 0.1μm/min but at an increased deposition rate of about 0.5μm/min. At such an increased deposition rate, the deposition time can be shortened.

[0038]

On the other hand, when the SiNx film being coarse in quality

provides a reduced insulating film function, a dense SiNx film is first deposited as an underlying layer at a typical deposition rate in a thickness of about 0.1μm, and then a thickness of about 1μm is deposited at an increased deposition rate, thereby making it possible to provide both the channel protecting and flattening functions.

[0039]

After the passivation film 9 and the organic interlayer film 26 are deposited, a contact hole 11 is provided at predetermined portions using a third mask. The ohmic contact layer 6 of n^+ a-Si doped with an impurity and a metal film such as of Cr, Ti, Mo, or Al are then deposited and patterned in a predetermined shape using a fourth mask, thus making it possible to fabricate the active matrix substrate having the structure of Fig. 5(d). Like in the first embodiment, it is also possible to form an n^+ layer by diffusing phosphorous into the surface of the intrinsic a-Si layer 5 instead of the ohmic contact layer 6.

[0040]

As described above, the fabrication method of this embodiment makes it possible to secure the protection of the intrinsic a-Si layer 5 as well as to reduce the shoulders of the TFT portion in addition to providing the effects of the first embodiment. Accordingly, a substrate flattened by the shoulders being reduced allows the surface of the alignment film to be also flattened, thereby making it possible to prevent disordered alignment of liquid crystal,

which otherwise occurs in the presence of the shoulder portions. For this reason, the fabrication method of this embodiment provides an effect of enabling the liquid crystal sandwiched between substrates to be aligned in a good condition.

[0041]

[Embodiment 3]

Referring to Figs. 6 to 8, described are a channel protective type active matrix substrate according to a third embodiment of the present invention and its fabrication method. Fig. 6 is a circuit diagram illustrating an active matrix substrate of the horizontal electric field system according to the third embodiment. Fig.7 is a plan view illustrating the fabrication steps of the active matrix substrate, with one pixel being extracted. Fig.8 is a sectional view illustrating the fabrication steps of the active matrix substrate, with the left side in the figure showing a gate terminal portion (a cross sectional view taken along the line E-E' of Fig. 6), the center showing a pixel portion (a cross sectional view taken along the line G-G' of Fig. 7), and the right side showing a drain terminal portion (a cross sectional view taken along the line F-F' of Fig. 6). Fig.8 is a sectional view illustrating the electrodes connected to the active matrix substrate.

[0042]

This embodiment is different from the first embodiment in that in this embodiment, the fabrication method according to the present invention is applied to an active matrix substrate of the horizontal

electric field system that employs an electric field between a common electrode 3 and the pixel electrode 10, which are formed in an interdigitated shape, to control the alignment of liquid crystal, and basically the same as that of the first embodiment.

[0043]

A method for fabricating the active matrix substrate of the horizontal electric field system will be described with reference to Figs. 7 and 8. First, as shown in Fig. 8(a), a metal film such as of Cr, Ti, Mo, or Al serving as the common electrode 3 and the gate electrode 2 is deposited on the transparent insulative substrate 1, for example, by sputtering in that order in a thickness of about 0.1 to 0.3μm. Then, using a first mask, a patterned resist is formed on the region serving as the common electrode 3, the drain electrode 7, and the drain conductor trace 14, and then an unnecessary metal film is removed by wet etching.

[0044]

Then, the gate insulating film 4 such as of SiNx and the intrinsic a-Si layer 5 serving as a semiconductor layer are successively deposited on the entire surface of the transparent insulative substrate 1 by plasma CVD or the like. Preferably, the SiNx has a thickness of about 0.3 to 0.5μm and the intrinsic a-Si has a thickness of about 0.05 to 0.2μm. After the deposition, using a second mask, a patterned resist is formed so as to cover the gate electrode 2, and an unnecessary intrinsic a-Si layer 5 and gate insulating film 4 are removed by dry etching, thereby providing the structure as

shown in Figs. 7(b) and 8(b).

[0045]

Then, the passivation film 9 such as of SiNx serving as channel protective film for the TFT is deposited on the entire surface of the substrate 1 by plasma CVD, for example, in a thickness of about 0.1 to 0.4μm. Subsequently, a third mask having openings at the source/drain junction on the intrinsic a-Si layer 5 and at the gate terminal portion is used to form a patterned resist, and the passivation film 9 is removed by dry etching or by wet etching, thereby providing the structure of Figs. 7(c) and 8(c).

[0046]

Then, to provide an ohmic contact with the intrinsic a-Si layer 5, the ohmic contact layer 6 of an n^+ a-Si layer doped with an impurity is deposited by CVD, for example, in a thickness of 20 to 100nm. Subsequently, a metal film such as of Cr, Mo, or Ti serving as the source/drain electrodes 7, 8 is deposited by sputtering, for example, in a thickness of about 0.1 to 0.3μm. As a method for obtaining an ohmic contact with the intrinsic a-Si layer 5, like in the first embodiment, it is also possible to allow phosphorus to diffuse into the intrinsic a-Si layer 5 to form an n^+ layer in place of forming the ohmic contact layer 6.

[0047]

Then, finally, using a fourth mask, an unnecessary source/drain metal film is etched to fabricate the channel protective type active matrix substrate of the horizontal electric field system having

the structure of Figs. 7(d) and 8(d).

[0048]

As described above, like in the first embodiment, the fabrication method according to this embodiment makes it possible to employ only four masks to form an active matrix substrate of the horizontal electric field system, with the surface and sidewalls of the intrinsic a-Si layer 5 being completely covered with the passivation film 9. When compared with the prior art fabrication method, the method according to this embodiment makes it possible to simplify the process by eliminating at least one PR.

[0049]

Furthermore, since an unnecessary gate insulating film 4 is removed in the step of Fig. 7(b), the connection between a common conductor trace 13 and the gate conductor trace 12, the gate electrode 2 and the drain conductor trace 14, and the gate conductor trace 12 and the source electrode 8 are constructed as shown in Figs. 9(a) and 9(b), when fabricated by the method according to this embodiment. Thus, when compared with the prior art structure shown in Figs. 15(a) and 15(b), this embodiment can provide shallow contact holes due to the absence of the gate insulating film 4, thereby providing an effect of facilitating connection.

[0050]

Furthermore, like the second embodiment, this embodiment makes it possible to achieve flatness by increasing the thickness of the passivation film, by modifying the conditions for depositing SiNx

as appropriate, or by stacking films of different materials in layers.

[0051]

[Embodiment 4]

Now, referring to Figs. 10 to 12, described are a channel protective type active matrix substrate of the horizontal electric field system according to a fourth embodiment of the present invention and its fabrication method. Fig. 10 is a plan view illustrating the fabrication steps of the active matrix substrate, with one pixel being extracted. Fig.11 is a sectional view illustrating the fabrication steps of the active matrix substrate, with the left side in the figure showing a gate terminal portion (a cross sectional view taken along the line E-E' of Fig. 6), the center showing a pixel portion (a cross sectional view taken along the line H-H' of Fig. 7), and the right side showing a drain terminal portion (a cross sectional view taken along the line F-F' of Fig. 6). Fig.12 is a sectional view illustrating the electrodes connected to the active matrix substrate. This embodiment is different from the third embodiment in that the gate insulating layer is allowed to remain on the entire surface of the substrate, with the other fabrication conditions being the same as those of the third embodiment.

[0052]

A method for fabricating the active matrix substrate of the horizontal electric field system will be described with reference to Figs. 10 and 11. First, like in the third embodiment, a metal film such as of Cr, Ti, Mo, or Al serving as the common electrode

3 and the gate electrode 2 are deposited on the transparent insulative substrate 1 by sputtering in that order in a thickness of about 0.1 to 0.3μm, and then patterned using a first mask.

[0053]

Then, the gate insulating film 4 such as of SiNx and the intrinsic a-Si layer 5 serving as a semiconductor layer are successively deposited on the entire surface of the substrate 1 by plasma CVD or the like in a thickness of about 0.3 to 0.5μm and about 0.05 to 0.2μm, respectively. In this embodiment, after the deposition, using a second mask, the intrinsic a-Si layer 5 is etched to remain only on the gate electrode 2 with the gate insulating film 4 allowed to remain on the entire surface of the substrate 1, thereby providing the structure as shown in Figs. 10(b) and 11(b).

[0054]

Then, the passivation film 9 such as of SiNx serving as channel protective film for the TFT is deposited on the entire surface of the substrate 1 by plasma CVD in a thickness of about 0.1 to 0.4μm. Subsequently, a third mask is used to remove the passivation film of the source/drain junction on the intrinsic a-Si layer 5 and the openings of the gate and drain terminal portions. However, in this embodiment, since the gate insulating film 4 also remains on the gate and drain terminal portions, this gate insulating film 4 is also removed by etching, thereby providing the structure of Figs. 10(c) and 11(c).

[0055]

Then, to provide an ohmic contact with the intrinsic a-Si layer 5, the ohmic contact layer 6 of an n^+ a-Si is deposited by CVD in a thickness of 20 to 100nm. Subsequently, a metal film such as of Cr, Mo, Ti, or Al serving as the source/drain electrodes 7, 8 is deposited by sputtering in a thickness of about 0.1 to 0.3μm. As a method for obtaining an ohmic contact with the intrinsic a-Si layer 5, like in the third embodiment, it is also possible to allow phosphorus or the like to diffuse into the surface of the intrinsic a-Si layer 5 to provide the same effects.

[0056]

Then, finally, using a fourth mask, an unnecessary source/drain metal film is etched to provide a fabricated channel protective type active matrix substrate of the horizontal electric field system having the structure of Fig. 11(d).

[0057]

As described above, like in the third embodiment, the fabrication method according to this embodiment makes it possible to employ only four masks to form an active matrix substrate of the horizontal electric field system, with the surface and sidewalls of the intrinsic a-Si layer 5 being completely covered with the passivation film 9. When compared with the prior art fabrication method, this method makes it possible to simplify the process by eliminating at least one PR.

[0058]

Furthermore, the connection between the common conductor trace

13 and the gate conductor trace 12, the gate electrode 2 and the drain conductor trace 14, and the gate conductor trace 12 and the source electrode 8 are as shown in Figs. 12(a) and 12(b), when fabricated by the method according to this embodiment. Thus, when compared with the third embodiment, this embodiment provides an interlayer film thicker by the amount of the remaining gate insulating film, however, this provides an effect of reducing the short-circuit between the gate and the drain.

[0059]

[Effects of the Invention]

As described above, the present invention can provide effects of using only four masks to fabricate a channel protective type active matrix substrate with the intrinsic a-Si semiconductor layer being completely covered with a channel protective film, thereby realizing an active matrix substrate at lower costs.

[0060]

This is because the gate insulating film and the a-Si semiconductor layer are collectively etched using the same mask and then a passivation film is deposited, thereby making it possible to reduce the number of steps and as well completely cover the a-Si semiconductor layer with the passivation film.

[0061]

Furthermore, the present invention can also make the shoulders of the TFT smaller by optimizing the thickness of the passivation film as appropriate, thereby having an effect of providing a uniform

alignment to the liquid crystal sandwiched between the opposing substrates.

[0062]

Additionally, the present invention also provides an active matrix substrate on which a storage capacitor, a protective element for preventing electrostatic damage, openings at the gate and drain terminals, and transfer pads for the common electrode and openings for the terminal thereof are all formed.

[Brief Explanation of the Drawings]

[Fig. 1]

Fig.1 is a circuit diagram illustrating an active matrix substrate for a TN liquid crystal display device according to a first embodiment of the present invention.

[Fig. 2]

Fig.2 is a schematic plan view illustrating the fabrication steps of the active matrix substrate according to the first embodiment of the present invention.

[Fig. 3]

Fig.3 is a schematic sectional view illustrating the fabrication steps of the active matrix substrate according to the first embodiment of the present invention.

[Fig. 4]

Fig.4 is a sectional view illustrating the structure of a capacitive portion and a conductor trace connection of the active matrix substrate according to the first embodiment of the present

invention.

[Fig. 5]

Fig.5 is a schematic sectional view illustrating the fabrication steps of an active matrix substrate according to a second embodiment of the present invention.

[Fig. 6]

Fig.6 is a circuit diagram illustrating an active matrix substrate for a TN liquid crystal display device according to a third embodiment of the present invention.

[Fig. 7]

Fig.7 is a schematic plan view illustrating the fabrication steps of the active matrix substrate according to the third embodiment of the present invention.

[Fig. 8]

Fig.8 is a schematic sectional view illustrating the fabrication steps of the active matrix substrate according to the third embodiment of the present invention.

[Fig. 9]

Fig.9 is a sectional view illustrating the structure of a conductor trace connection of the active matrix substrate according to the third embodiment of the present invention.

[Fig. 10]

Fig.10 is a schematic plan view illustrating the fabrication steps of an active matrix substrate according to a fourth embodiment of the present invention.

[Fig. 11]

Fig.11 is a schematic sectional view illustrating the fabrication steps of the active matrix substrate according to the fourth embodiment of the present invention.

[Fig. 12]

Fig.12 is a sectional view illustrating the structure of a conductor trace connection of the active matrix substrate according to the fourth embodiment of the present invention.

[Fig. 13]

Fig.13 is a schematic sectional view illustrating the fabrication steps of a prior art active matrix substrate.

[Fig. 14]

Fig.14 is a sectional view illustrating the structure of a capacitive portion and a conductor trace connection of the prior art active matrix substrate.

[Fig. 15]

Fig.15 is a sectional view illustrating the structure of the conductor trace connection of the prior art active matrix substrate.

[Explanation of Letters or Numerals]

1: Transparent insulative substrate

2: Gate electrode

2a: Lower gate electrode (ITO layer)

2b: Upper gate electrode (metal layer)

3: Common electrode

4: Gate insulating film

5: Intrinsic a-Si layer

6: Ohmic contact layer (n^+ a-Si layer)

7: Drain electrode

8: Source electrode

9: Passivation film

10: Pixel electrode

11: Contact hole

12: Gate conductor trace

12a: Lower gate conductor trace (ITO layer)

12b: Upper gate conductor trace (metal layer)

13: Common conductor trace

14: Drain conductor trace

14a: Lower drain conductor trace (n^+ a-Si layer)

14b: Upper drain conductor trace (metal layer)

15: Gate terminal

16: Drain terminal

17: Thin film transistor for driving pixel

18: Protective transistor

19: Transfer pad for common electrode

20: Al oxide layer

21: Gate storage electrode

22: Common conductor trace connection layer

23: Source/drain conductor trace

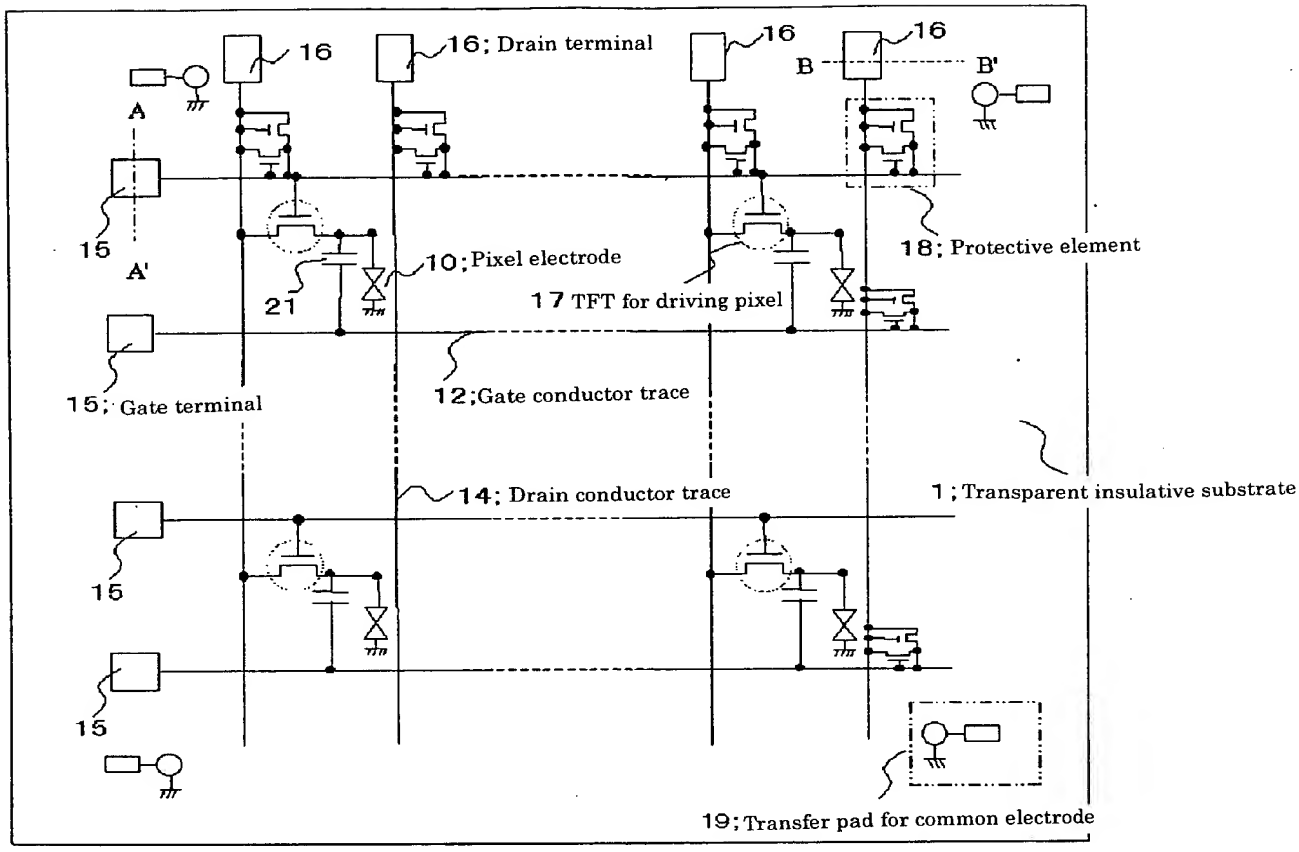
24: Connection conductor trace layer

25: Channel protective film

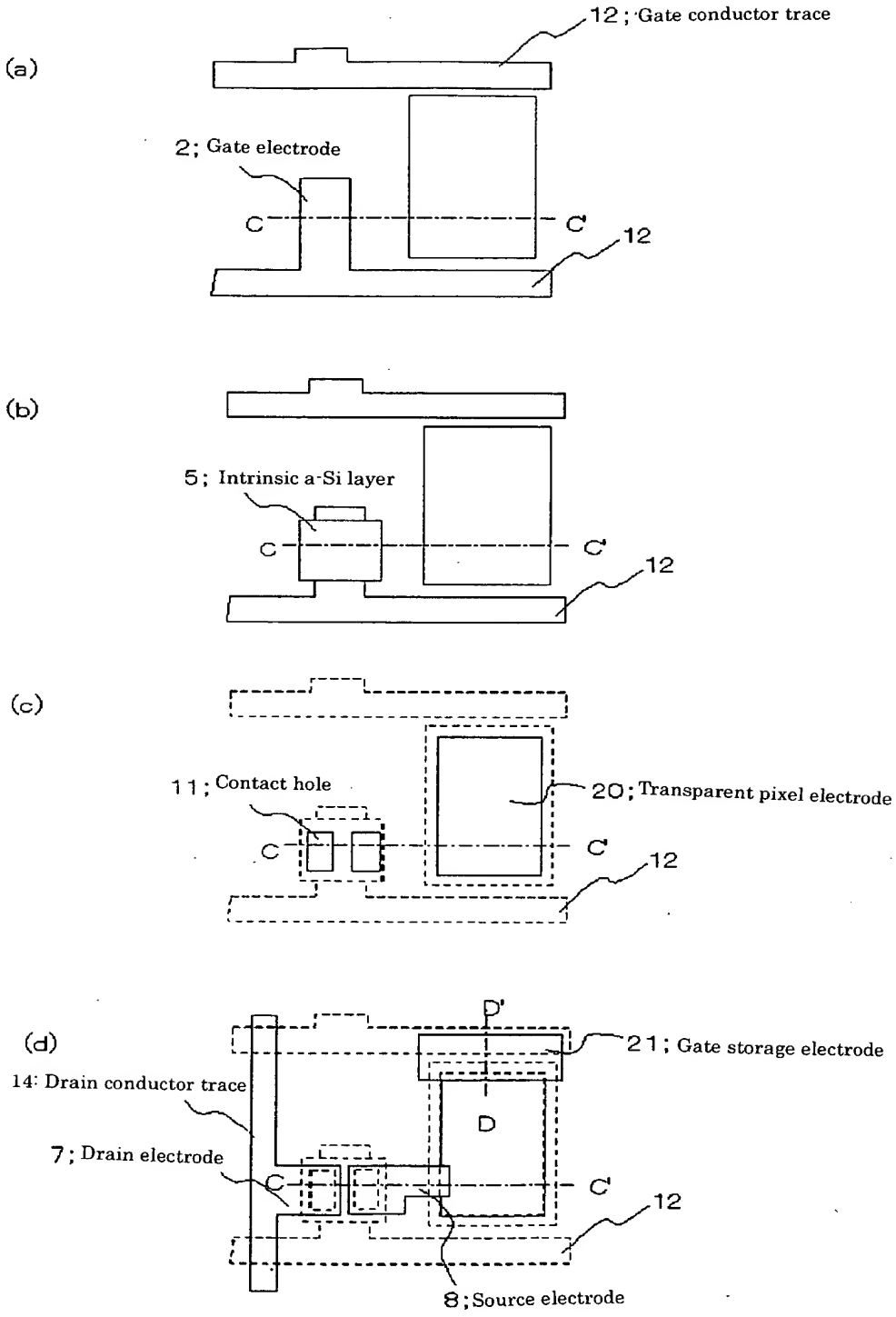
26: Organic interlayer film

[Name of the Document] Drawings

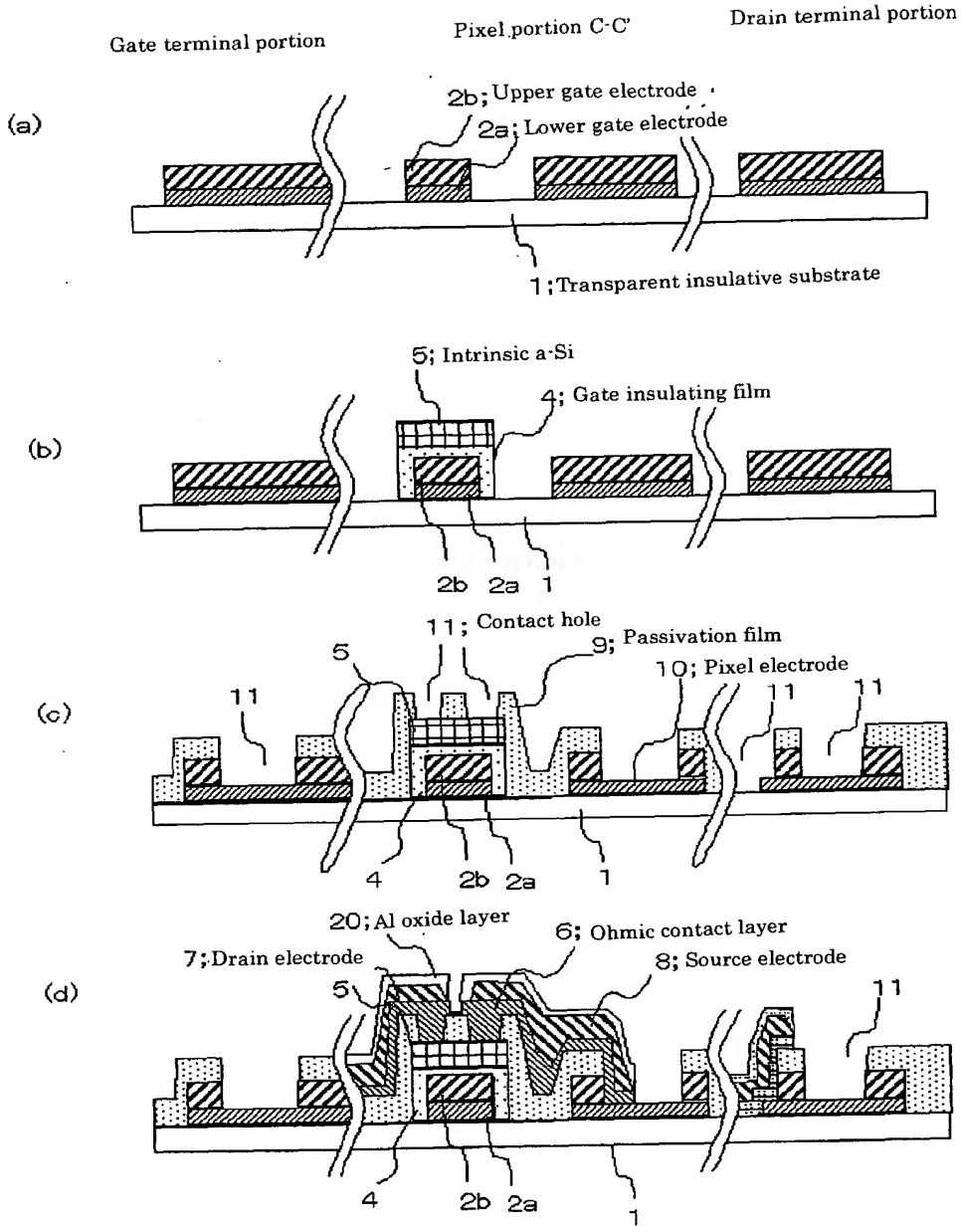
[Fig. 1]



[Fig. 2]

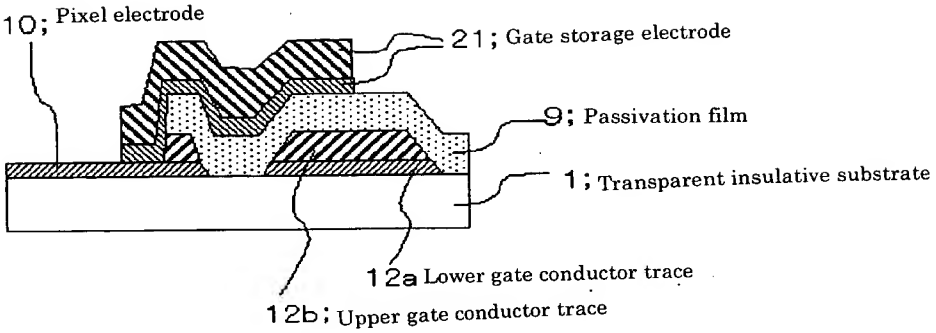

(a)
12; Gate conductor trace
2; Gate electrode
C
C'
12
(b)
5; Intrinsic a-Si layer
C
C'
12
(c)
11; Contact hole
20; Transparent pixel electrode
C
C'
12
(d)
P'
21; Gate storage electrode
14; Drain conductor trace
D
7; Drain electrode
C
C'
12
8; Source electrode

[Fig. 3]

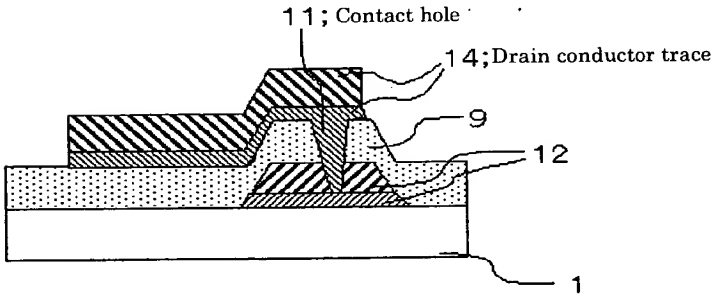

Gate terminal portion
Pixel portion C-C'
Drain terminal portion
(a)
2b; Upper gate electrode
2a; Lower gate electrode
1; Transparent insulative substrate
(b)
5; Intrinsic a-Si
4; Gate insulating film
2b 2a 1
(c)
11; Contact hole
9; Passivation film
10; Pixel electrode
5
11
11
11
4
2b 2a
1
(d)
20; Al oxide layer
6; Ohmic contact layer
7; Drain electrode
8; Source electrode
5
11
4
2b 2a
1

[Fig. 4]

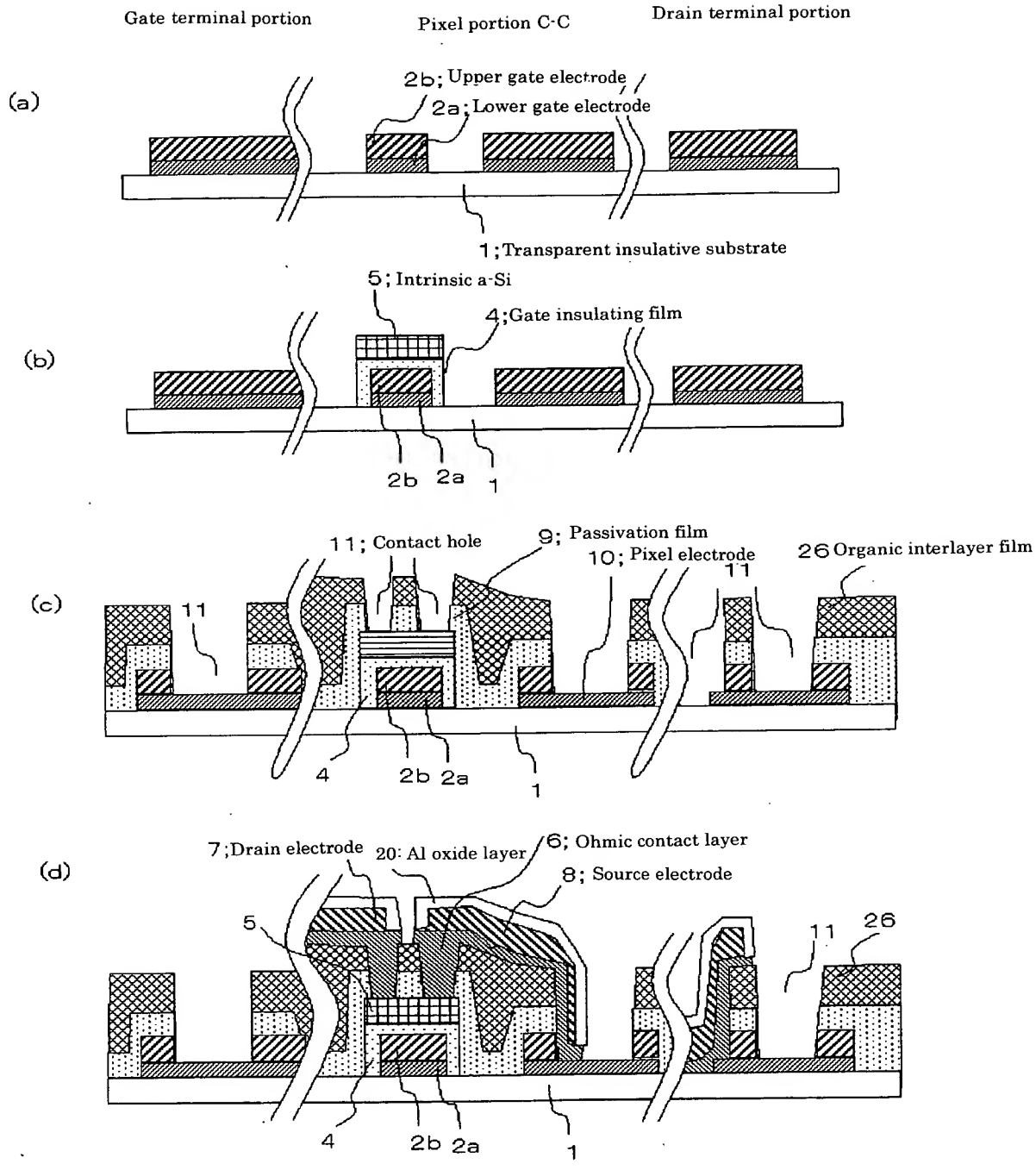
(a)


10; Pixel electrode
21; Gate storage electrode
9; Passivation film
1; Transparent insulative substrate
12a Lower gate conductor trace
12b; Upper gate conductor trace

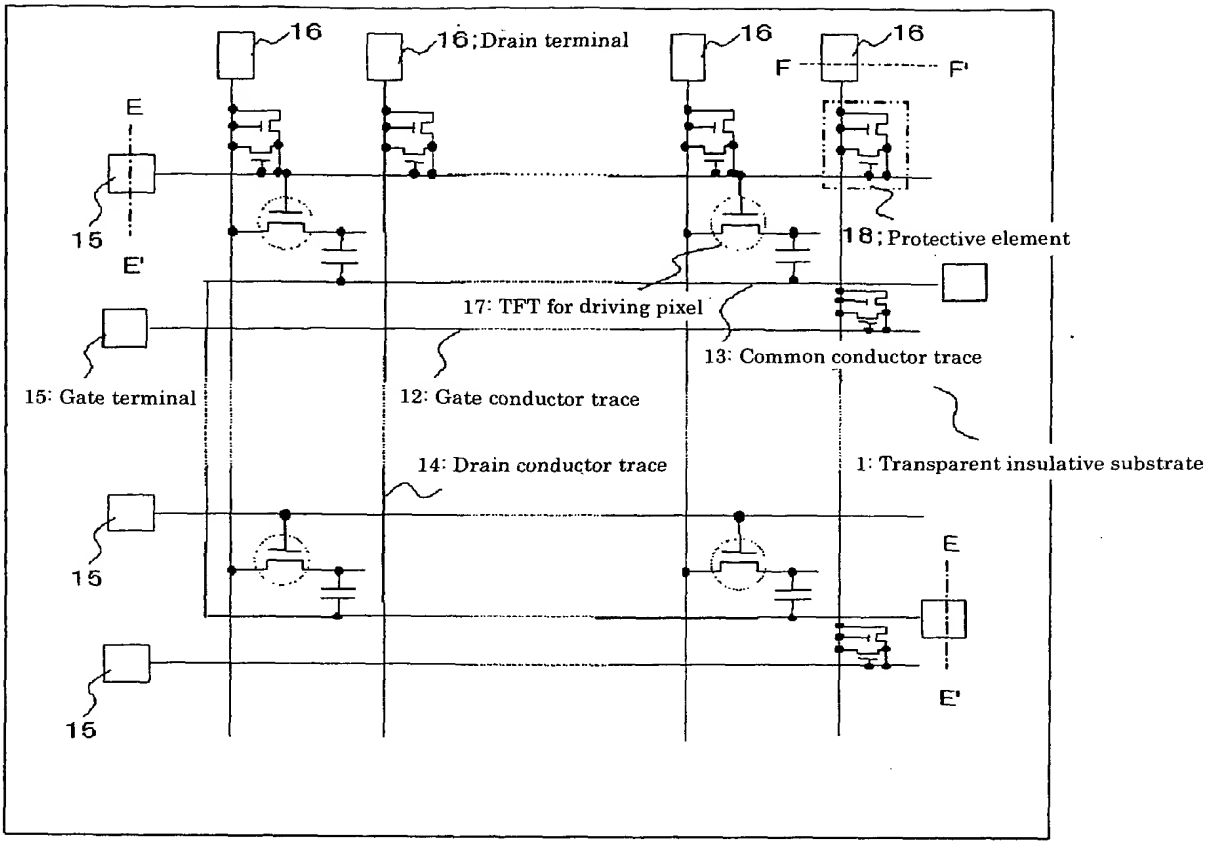
(b)


11; Contact hole
14;Drain conductor trace
9
12
1

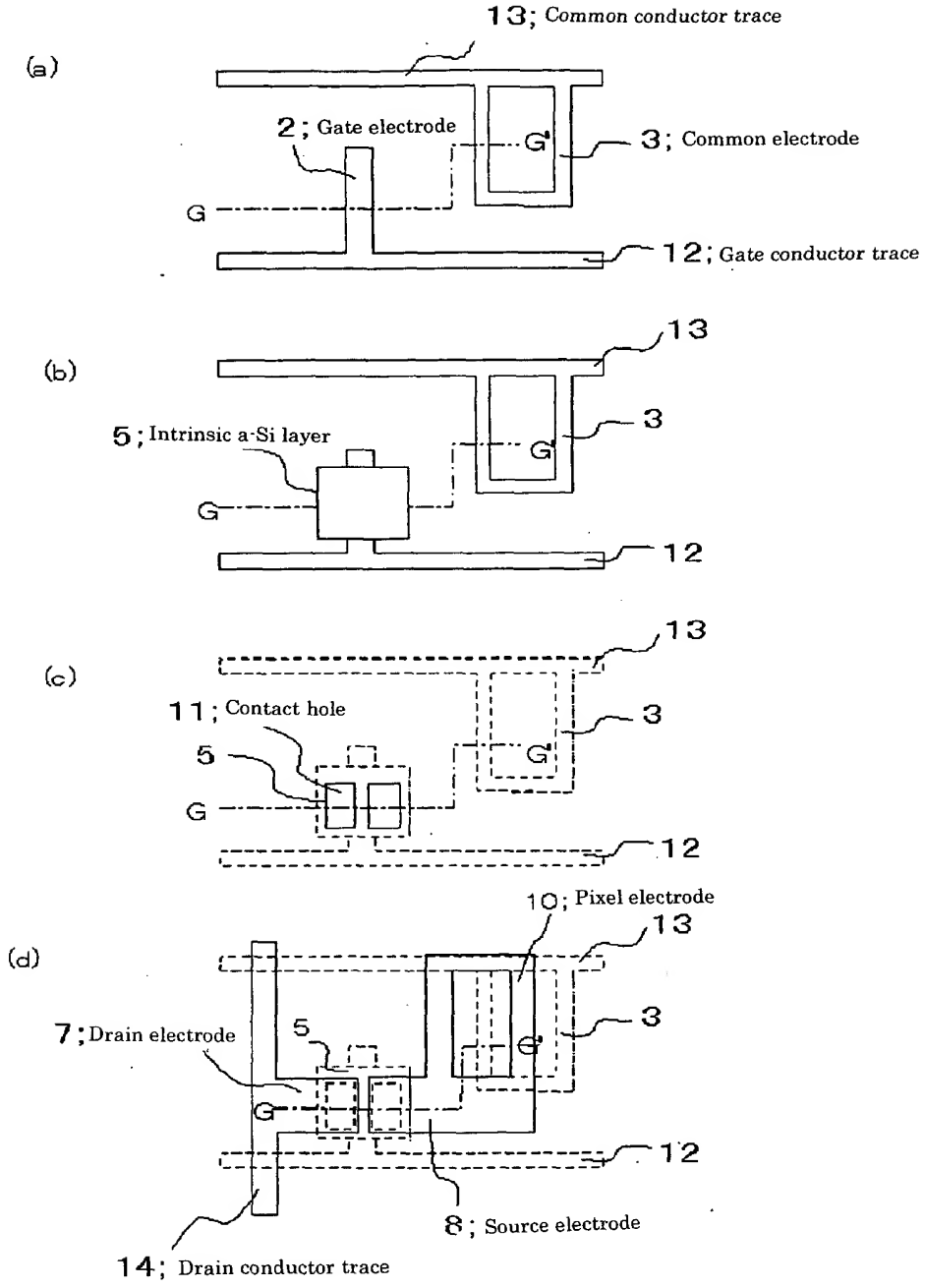
[Fig. 5]


Gate terminal portion
Pixel portion C-C
Drain terminal portion
(a)
2b; Upper gate electrode
2a; Lower gate electrode
1; Transparent insulative substrate
(b)
5; Intrinsic a-Si
4; Gate insulating film
2b 2a 1
(c)
11; Contact hole
9; Passivation film
10; Pixel electrode
26 Organic interlayer film
11
11
11
4
2b 2a
1
(d)
7; Drain electrode
20: Al oxide layer
6; Ohmic contact layer
8; Source electrode
5
11
26
4
2b 2a
1

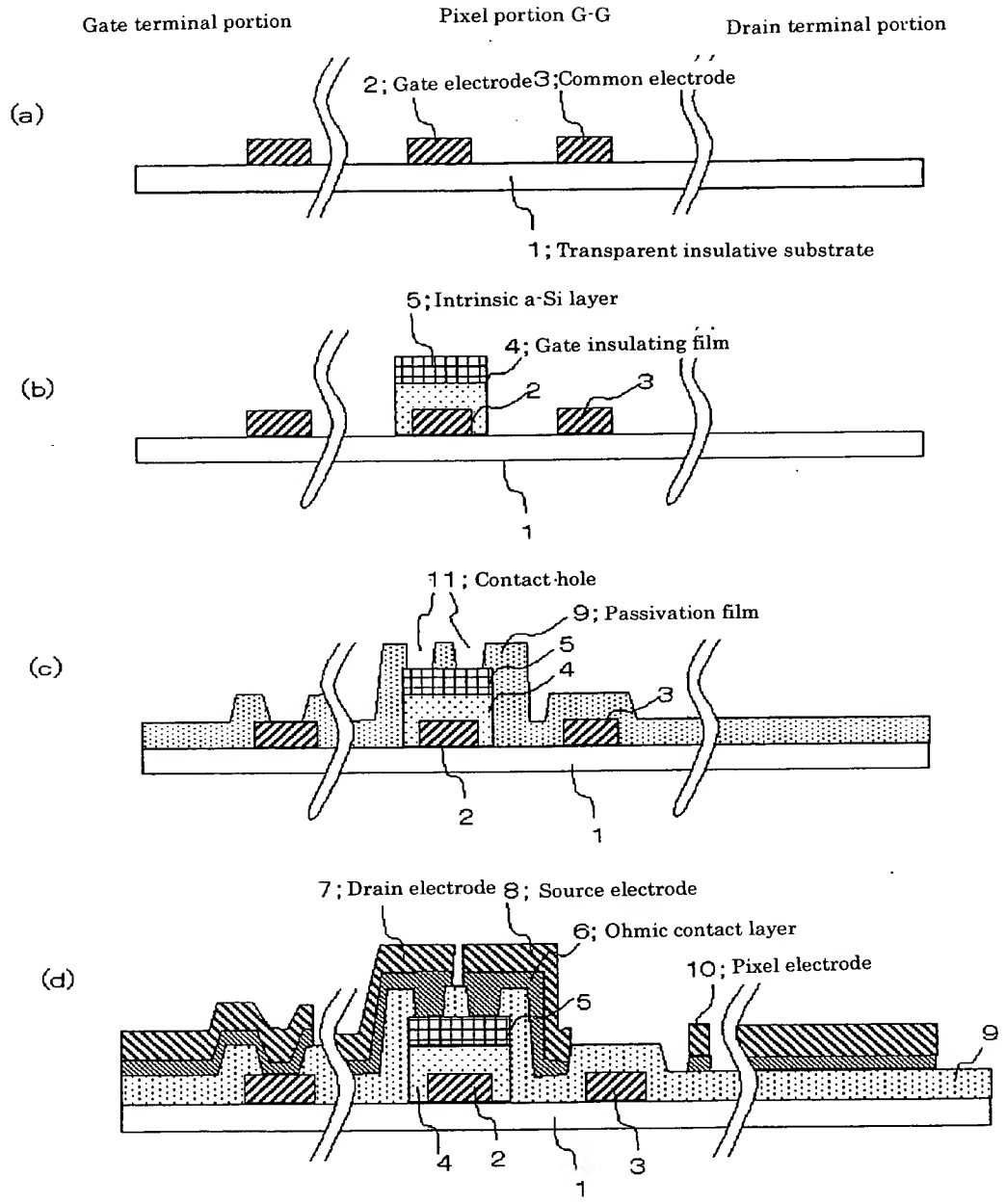
[Fig. 6]


16
16; Drain terminal
16
16
F
F'
E
15
E'
18; Protective element
17: TFT for driving pixel
13: Common conductor trace
15: Gate terminal
12: Gate conductor trace
1: Transparent insulative substrate
14: Drain conductor trace
15
E
15
E'

[Fig. 7]

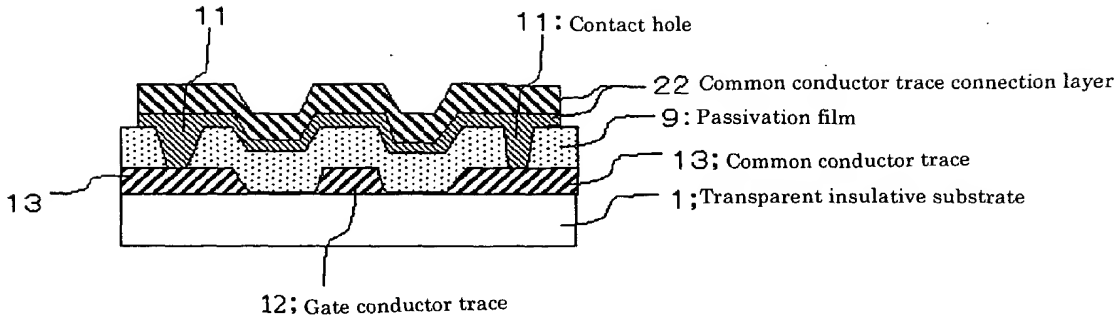

(a)
13; Common conductor trace
2; Gate electrode
G'
3; Common electrode
G
12; Gate conductor trace
(b)
13
3
5; Intrinsic a-Si layer
G'
G
12
(c)
13
11; Contact hole
3
5
G'
G
12
(d)
10; Pixel electrode
13
3
7; Drain electrode
5
G'
G
12
8; Source electrode
14; Drain conductor trace

[Fig. 8]

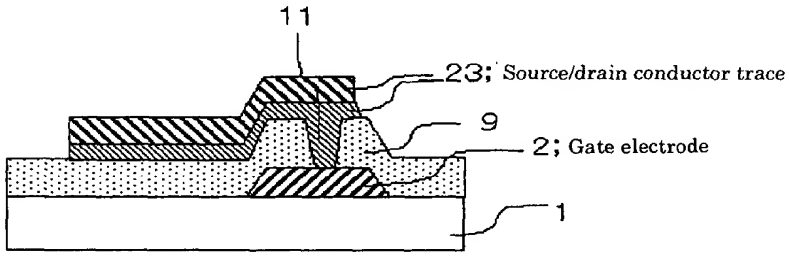

Gate terminal portion
Pixel portion G-G
Drain terminal portion
(a)
2; Gate electrode
3; Common electrode
1; Transparent insulative substrate
(b)
5; Intrinsic a-Si layer
4; Gate insulating film
2
3
1
(c)
11; Contact hole
9; Passivation film
5
4
3
2
1
(d)
7; Drain electrode
8; Source electrode
6; Ohmic contact layer
10; Pixel electrode
5
9
4
2
3
1

[Fig. 9]

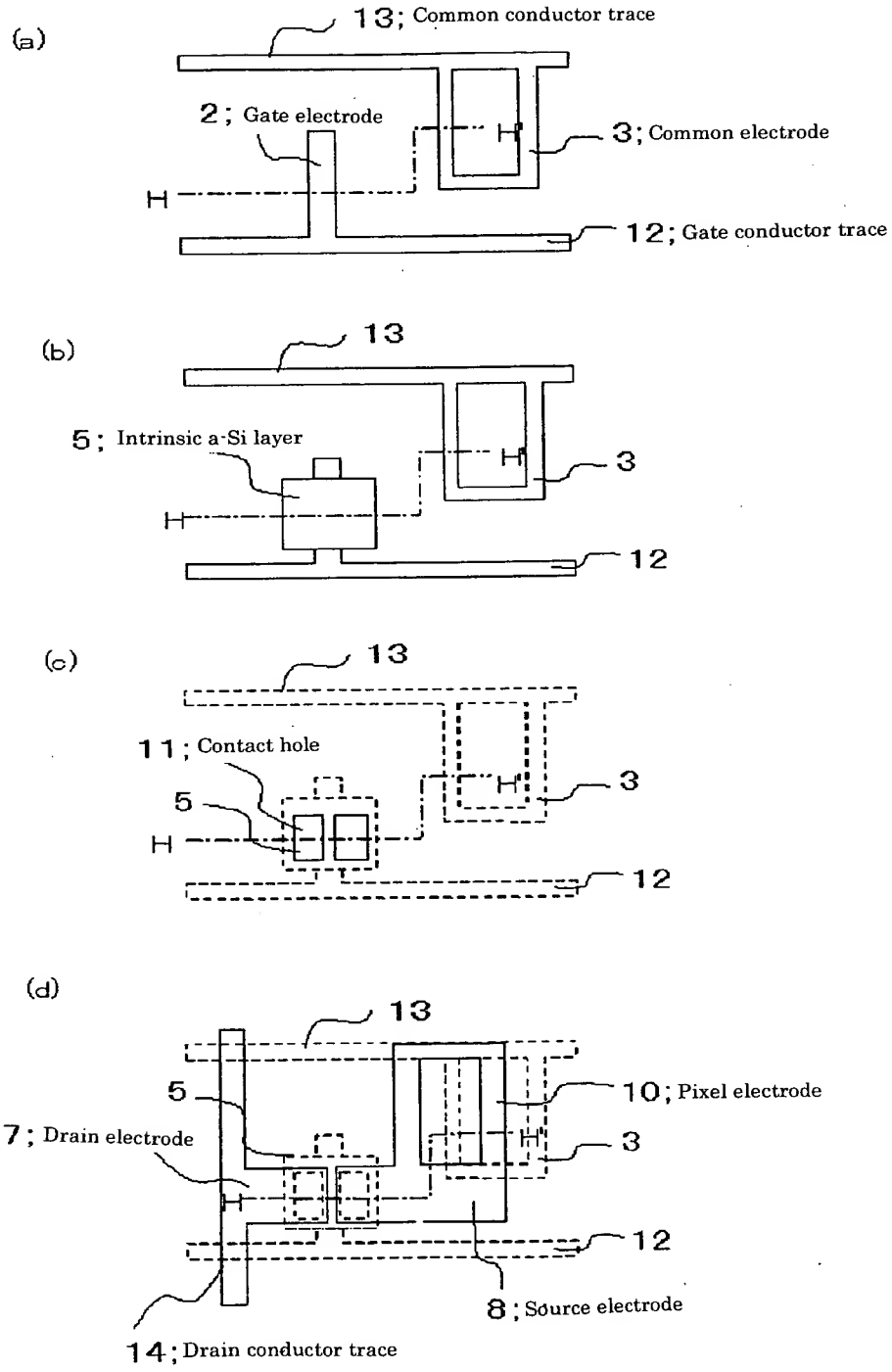
(a)


11
11: Contact hole
22 Common conductor trace connection layer
9: Passivation film
13; Common conductor trace
1 ;Transparent insulative substrate
13
12; Gate conductor trace

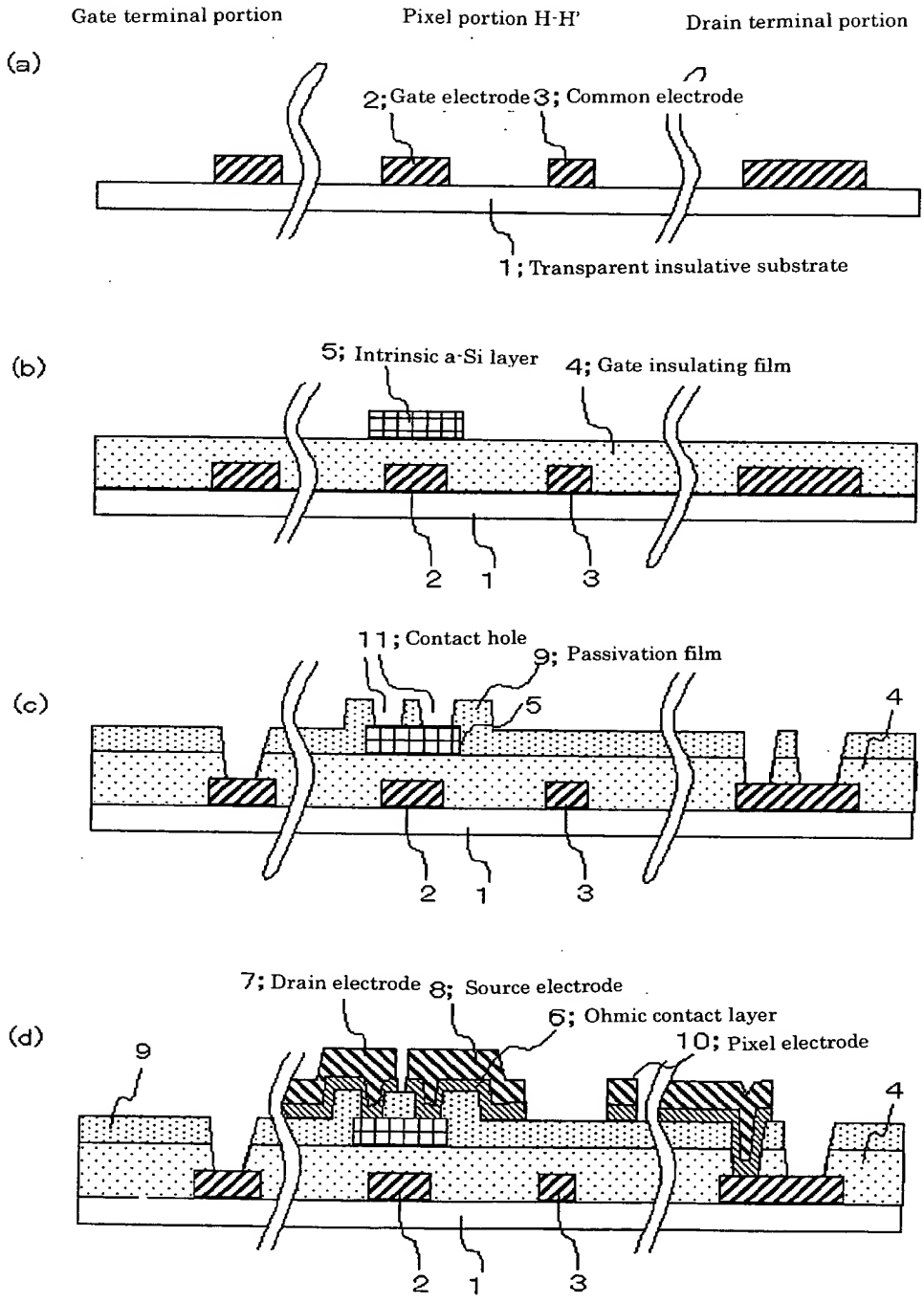
(b)


11
23; Source/drain conductor trace
9
2; Gate electrode
1

[Fig. 10]

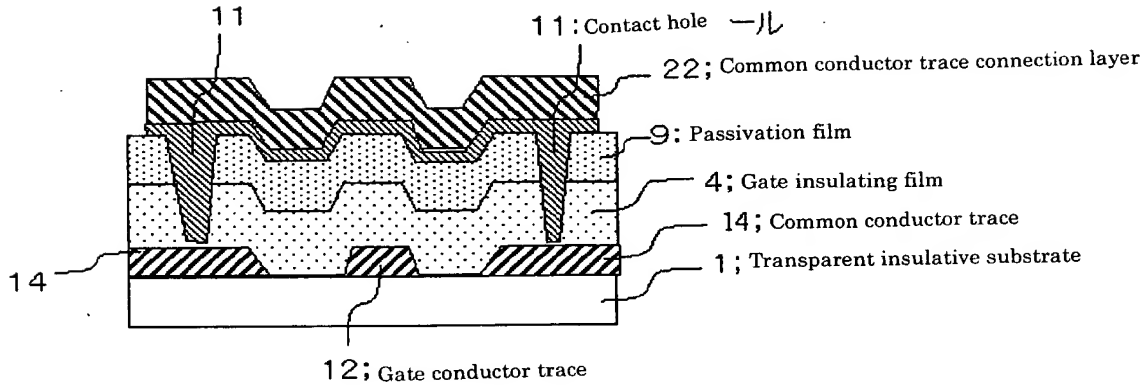

(a)
13; Common conductor trace
2; Gate electrode
3; Common electrode
H
H'
12; Gate conductor trace
(b)
13
5; Intrinsic a-Si layer
3
12
(c)
13
11; Contact hole
5
3
12
(d)
13
5
10; Pixel electrode
7; Drain electrode
3
12
8; Source electrode
14; Drain conductor trace

[Fig. 11]

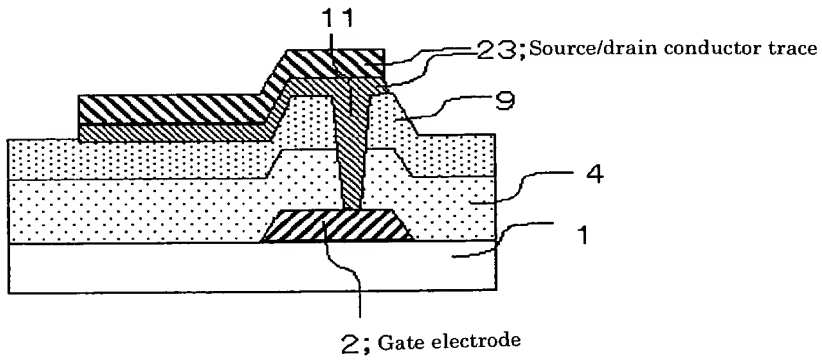

Gate terminal portion
Pixel portion H-H'
Drain terminal portion
(a)
2; Gate electrode
3; Common electrode
1; Transparent insulative substrate
(b)
5; Intrinsic a-Si layer
4; Gate insulating film
2
1
3
(c)
11; Contact hole
9; Passivation film
5
4
2
1
3
(d)
7; Drain electrode
8; Source electrode
6; Ohmic contact layer
10; Pixel electrode
9
4
2
1
3

[Fig. 12]

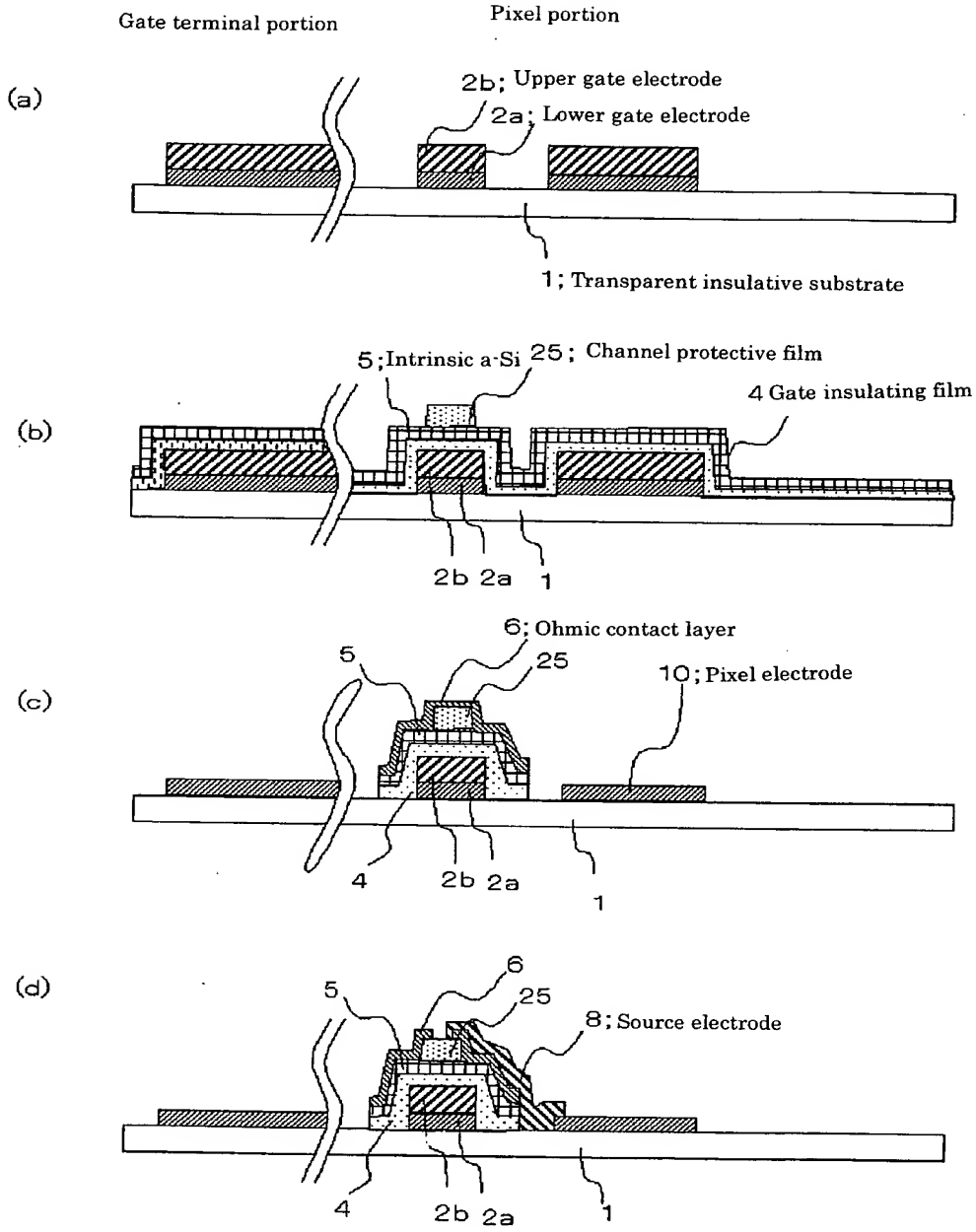
(a)


11
11: Contact hole
22; Common conductor trace connection layer
9: Passivation film
4; Gate insulating film
14; Common conductor trace
1; Transparent insulative substrate
14
12; Gate conductor trace

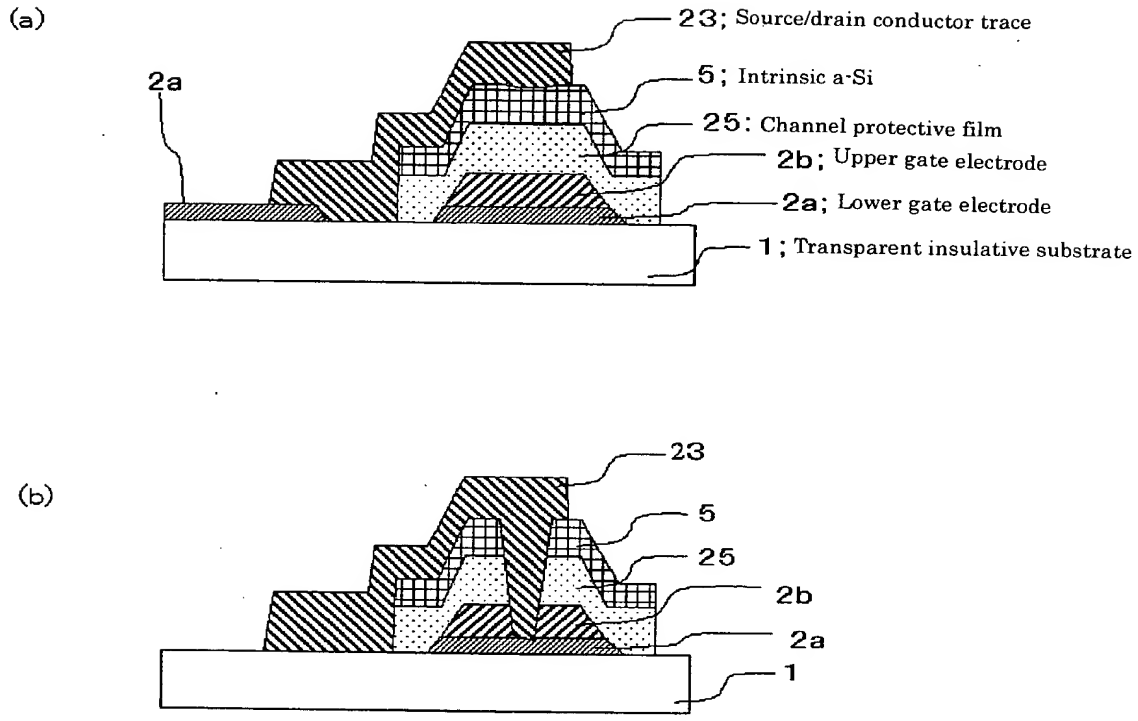
(b)


11
23; Source/drain conductor trace
9
4
1
2; Gate electrode

[Fig. 13]

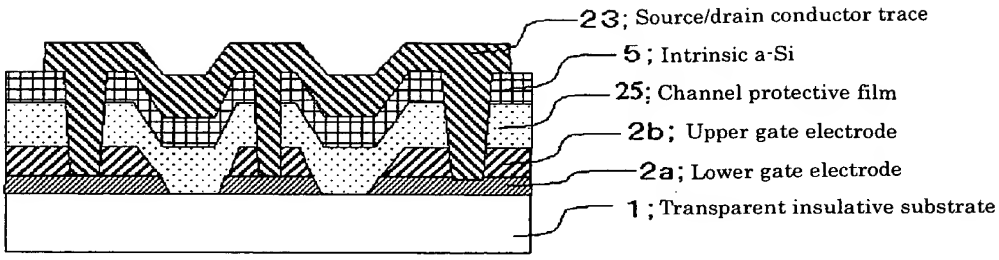

Gate terminal portion
Pixel portion
(a)
2b; Upper gate electrode
2a; Lower gate electrode
1; Transparent insulative substrate
(b)
5;Intrinsic a-Si
25; Channel protective film
4 Gate insulating film
2b 2a 1
(c)
6; Ohmic contact layer
5
25
10; Pixel electrode
4
2b 2a
1
(d)
6
5
25
8; Source electrode
4
2b 2a
1

[Fig. 14]

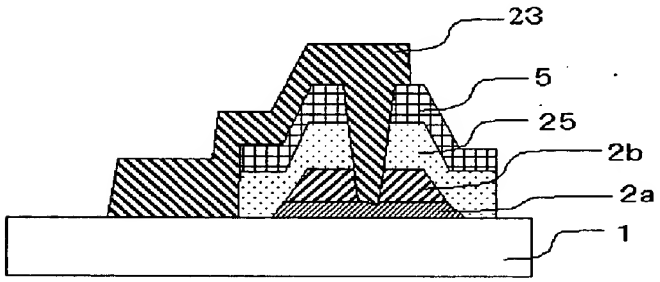

(a)
23; Source/drain conductor trace
5; Intrinsic a-Si
25: Channel protective film
2b; Upper gate electrode
2a; Lower gate electrode
1; Transparent insulative substrate
2a
(b)
23
5
25
2b
2a
1

[Fig. 15]

(a)


23; Source/drain conductor trace
5 ; Intrinsic a-Si
25; Channel protective film
2b; Upper gate electrode
2a; Lower gate electrode
1 ; Transparent insulative substrate

(b)


23
5
25
2b
2a
1

[Document Name] Abstract

[Abstract]

[Object]

To provide an active matrix substrate and its fabrication method, by which only four masks are employed to form a channel protective type active matrix substrate with the entire surface of an a-Si layer being covered with passivation film.

[Solving Means]

A transparent electrode and metal film are staked in layers on a transparent insulative substrate to form gate electrodes (2a, 2b in Fig. 3) and pixel electrodes using a first mask. On top thereof, gate insulating film (4 in Fig. 3) and an intrinsic amorphous silicon layer (5 in Fig. 3) are stacked in layers and formed collectively in a predetermined shape using a second mask, so that passivation film (9 in Fig. 3) deposited so as to cover a surface and sidewalls of the intrinsic amorphous silicon layer is provided with an opening. On top thereof, electrode layers (7 and 8 in Fig. 3) are deposited to form predetermined conductor traces using a fourth mask. Thus, using only four masks, an active matrix substrate of a channel protective type is fabricated which has the intrinsic amorphous silicon layer covered completely with the passivation film.

[Drawing Selected] Fig. 3